XC5200L
Field Programmable Gate Arrays

June 1, 1996 (Version 1.0)

Advance Product Specification

Features

- High-density family of Field-Programmable Gate Arrays (FPGAs)
- JEDEC-compliant 3.3 V version of XC5200 FPGA family
- Design- and process-optimized for low cost
  - 0.5-µm three-layer metal (TLM) process
- SRAM-based, in-system reprogrammable architecture
- Flexible architecture with abundant routing resources
  - VersaBlock™ logic module
  - VersaRing™ I/O interface
  - Dedicated cell-feedthrough path
  - Hierarchical interconnect structure
  - Extensive registers/latches
  - Dedicated carry logic for arithmetic functions
  - Cascade chain for wide input functions
  - Dedicated IEEE 1149.1 boundary-scan logic
  - Internal 3-state bussing capability
  - Four global low-skew clock or signal distribution nets
  - Output slew-rate control
  - 4-mA sink current per output
- Configured by loading binary file
  - Unlimited reprogrammability
  - Seven programming modes, including high-speed Express™ mode
- 100% factory tested
- 100% architecture, pin-out and bit-stream compatible with XC5200 families
- 100% footprint compatibility for common packages
- 5 V tolerant inputs
- Fully supported by XACT*step*™ Development System
  - Includes complete support for XACT-Performance™, X-BLOX™, Unified Libraries, Relationally Placed Macros (RPMs), XDelay, and XChecker™
  - Wide selection of PC and workstation platforms
  - Interfaces to more than 100 third-party CAE tools

Description

The XC5200L Field-Programmable Gate Array Family is engineered to deliver the lowest cost of any FPGA family. By optimizing the new XC5200L architecture for three-layer metal technology and 0.5-µm CMOS SRAM process, dramatic advances have been made in silicon efficiency. These advances position the XC5200L family as a cost-effective, high-volume alternative to gate arrays.

Building on experiences gained with three previous successful SRAM FPGA families, the XC5200L family brings a robust feature set to high-density programmable logic design. The VersaBlock logic module, the VersaRing I/O interface, and a rich hierarchy of interconnect resources combine to enhance design flexibility and reduce time-to-market.

Complete support for the XC5200L family is delivered through the familiar XACT*step* software environment. The XC5200L family is fully supported on popular workstation and PC platforms. Popular design entry methods are fully supported, including ABEL, schematic capture, and synthesis. Designers utilizing logic synthesis can use their existing Synopsys, Viewlogic, Mentor, and Exemplar tools to design with the XC5200L devices.

Table 1: Initial XC5200L Field-Programmable Gate Array Family Members

Device	XC5202L	XC5206L	XC5215L
Max Logic Gates	3,000	10,000	23,000
Typical Gate Range	2,000 - 3,000	6,000 - 10,000	15,000 - 23,000
VersaBlock Array	8 x 8	14 x 14	22 x 22
Number of CLBs	64	196	484
Number of Flip-Flops	256	784	1,936
Number of I/Os	84	148	244
TBUFs per Horizontal Longline	10	16	24

XC5200L Switching Characteristics

Xilinx maintains test specifications for each product as controlled documents. To insure the use of the most recently released device performance parameters, please request a copy of the current test-specification revision.

XC5200L Operating Conditions

Symbol	Description	Min	Max	Units
V_{CC}	Supply voltage relative to GND Commercial: T_J=0°C to 85°C junction	3.0	3.6	V
V_{IH}	High-level input voltage—CMOS configuration	2.0	5.0	V
V_{IL}	Low-level input voltage—CMOS configuration	-0.3	0.8	V
T_{IN}	Input signal transition time		250	ns

XC5200L DC Characteristics Over Operating Conditions

Symbol	Description	Min	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = -4 mA, V_{CC} min	2.4		V
V_{OL}	Low-level output voltage @ I_{OL} = 4 mA, V_{CC} max (Note 1)		0.4	V
I_{CCO}	Quiescent FPGA supply current (Note 2)		N/A	mA
I_{IL}	Leakage current	-10	+10	µA
C_{IN}	Input capacitance (sample tested)		15	pF
I_{RIN}	Pad pull-up (when selected) @ V_{IN} = 0V (sample tested)	0.02	0.25	mA

Notes: 1. With 50% of the outputs simultaneously sinking 12mA, up to a maximum of 64 pins.
2. With no output current loads, all package pins at Vcc or GND, either TTL or CMOS inputs, and the FPGA configured with a MakeBits tie option.

XC5200L Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	-0.5 to +7.0	V
V_{IN}	Input voltage with respect to GND	-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	-0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)	+260	°C
T_J	Junction temperature in plastic packages	+125	°C
	Junction temperature in ceramic packages	+150	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.