All-SiC Module for Mega-Solar Power Conditioner

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ABSTRACT

An all-SiC module for mega-solar power conditioners has been developed. The structure developed for the all-SiC module has achieved a reduction in circuit inductance of approximately 80% from the existing structure that uses wire bonding. This allows for a significant reduction in loss, leading to an advantage in high-speed switching of SiC devices. In addition, it has shown a higher capability to thermal load in a power cycling test as compared with the conventional structure. We have developed an all-SiC chopper module for booster circuits by applying these technologies and integrated it in a mega-solar power conditioner, thereby achieving the world's highest level of efficiency of 98.8%.

1. Introduction

To realize a low carbon society, there has been a growing need to utilize renewable energy and save energy. Above all, power conversion technology is becoming increasingly important to efficiently use electric power, which is essential to our lives. In power conversion, power semiconductors play an important role. Recently, as next-generation semiconductors that replace silicon (Si) devices, which were the mainstream of power semiconductors, research and development efforts are actively in progress for power semiconductors that use wide-bandgap semiconductors of silicon carbide (SiC), gallium nitride (GaN), etc. Among them, SiC devices are increasingly being adopted for familiar power electronics products including consumer electronics as well as the industrial field and they are expected to be applied to an even wider range of products such as hybrid electric vehicles (HEVs) and electric vehicles (EVs).

This paper describes the technologies used for an all-SiC module equipped with SiC-metal-oxide-semiconductor field-effect transistor (SiC-MOSFET) and SiC-Schottky barrier diode (SiC-SBD) and application to a power conditioner (PCS) for mega-solar plants.

2. Characteristics of All-SiC Module

2.1 Module structure

Figure 1 shows cross-sectional views of modules with the developed and conventional structures. The structure developed for the all-SiC module greatly differs from that for conventional Si-insulated-gate bipolar transistor (Si-IGBT) modules. In the developed structure, copper pins formed on the power substrate are used for interconnection instead of the conventional aluminum bonding wire. This allows a large current to be run and in turn high-density mounting of SiC devices. As the isolation substrate on which to mount the chip, in place of the conventional direct copper bonding (DCB) substrate, a Si_3N_4 (silicon nitride) ceramic substrate joined with a thick copper block is used for reducing thermal resistance. In addition, as the encapsulation material in the module, epoxy resin is used in place of the conventional silicone gel to ensure high reliability in high-temperature operation.

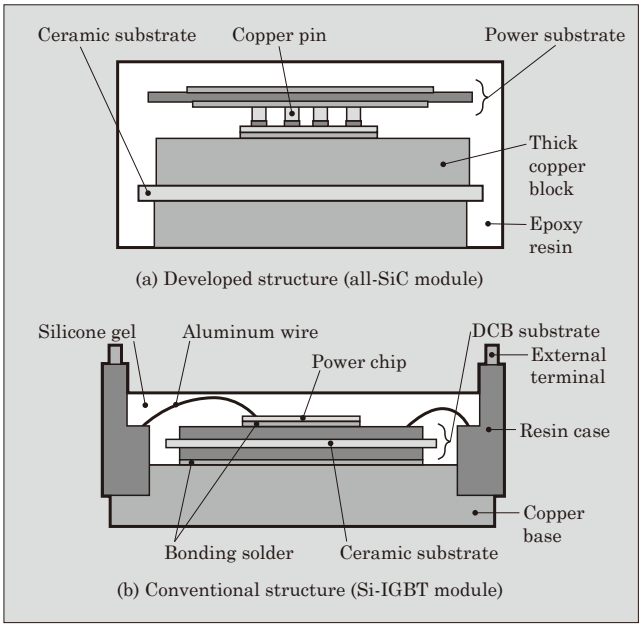

Fig.1 Cross-sectional views of modules

Figure 2 is a photo of the appearance of the all-SiC module in the new package and Si-IGBT module in the

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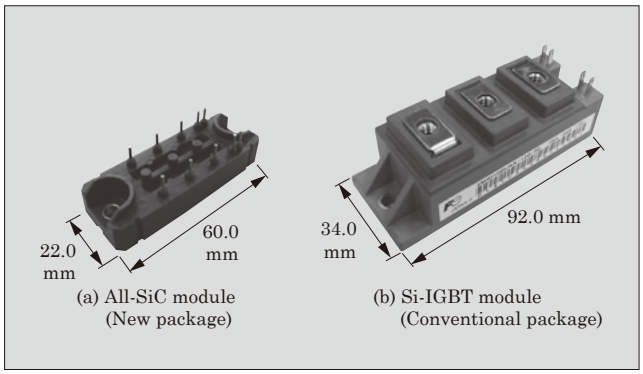

Fig.2 Appearance of modules

conventional package. Both modules have a rating of 1,200 V/100 A. The footprint of the new package has been reduced to approximately 40% of the conventional package.

2.2 Low-inductance design

(1) Inductance evaluation

As compared with Si-IGBT used for current power modules, SiC-MOSFET is capable of switching at a higher speed. However, because surge voltage generally increases in proportion to the switching speed, lowering the inductance of circuit in the module is important for reducing the impact of noise on gate signals.

Figure 3 shows a comparison of inductance between the gate circuit and main circuit. The comparison is based on the respective internal inductance of the gate circuit and main circuit determined by simulation with the conventional package, which is specified as 1. First, the inductance of the gate circuit has been confirmed to be reduced by approximately 80% from the conventional package. The same evaluation has also been conducted with the main circuit, which has verified that the new package achieves an approximately 80% reduction from the conventional package both in analysis and actual measurement.

These results show that, in the new package, the current pathways have been shortened by miniaturizing the module with the power substrate and a low-thermal-resistance isolation substrate, that significantly contributes to reducing the inductance. In addition, the power substrate and thick copper block are arranged in parallel and the magnetic field interactions between the current pathways reduces the inductance.

(2) Loss comparison

In order to verify the effect of the lower inductance of the all-SiC module, modules with the same SiC devices mounted in the new and conventional packages have been built to conduct a switching test. As shown in Fig. 4, the new package has achieved an approximately 50% reduction in the switching loss as compared with the conventional package. This is because of the surge voltage suppression effect of the new package with lower inductance.

Figure 5 shows a comparison of the total loss in the switching frequency range from 10 to 100 kHz. The total loss consists of the switching loss and on-state loss and the comparison is based on the total loss at 10 kHz with SiC-MOSFET mounted in the conventional package, which is specified as 1. With the conventional package, the switching loss increase becomes larger with a higher switching frequency and the total loss at 100 kHz is 2.2. Meanwhile, the loss increase is smaller

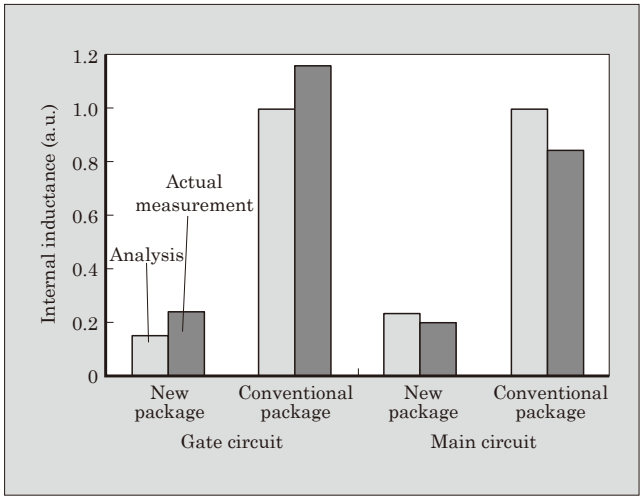

Fig.3 Inductance of gate circuit and main circuit

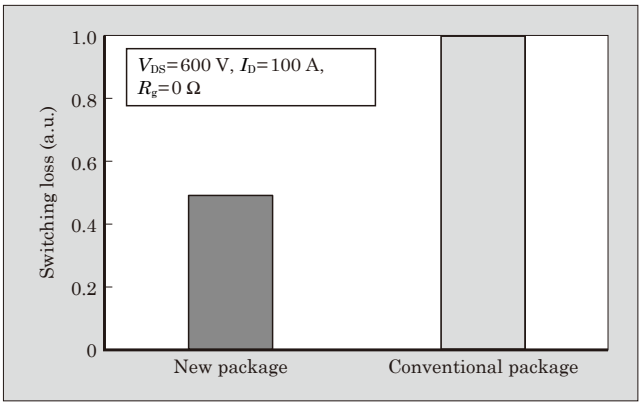

Fig.4 Switching loss of modules with SiC devices

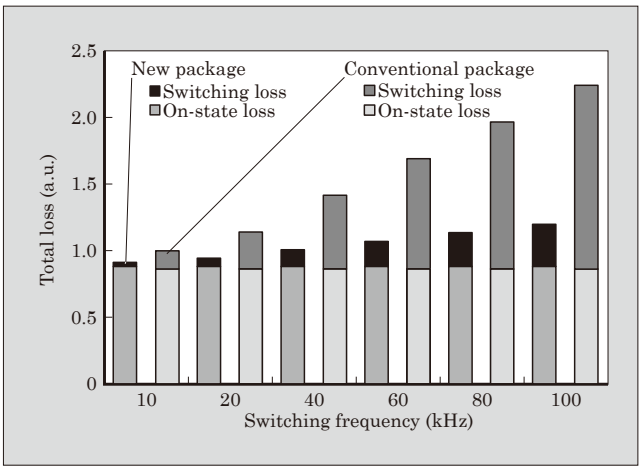

Fig.5 Total loss

with the new package and limited at 1.2. Focusing on the breakdown of the loss, the on-state loss is almost the same between the conventional and new packages and no frequency dependence is observed. In addition, the switching loss with the conventional package is more than 4 times higher than with the new package at any of the frequencies, which shows that it accounts for a larger proportion of the entire loss as the frequency increases. In this way, the new package, which has successfully reduced the internal inductance of the module, has been confirmed to be advantageous for high-speed switching of SiC devices.

2.3 High reliability

(1) ΔT_j power cycling test

In a power module, thermal stress is generated by temperature rise during device operation, which may cause breakage of a chip junction, etc. A ΔT_j power cycling test is a reliability test for evaluating the lifetime of a power module by repeating this device operation.

Figure 6 shows a comparison of ΔT_j power cycling test lifetime. With the test starting temperature at 25ºC, the figure plots the temperature amplitude ΔT_j along the horizontal axis and the number of cycles with a cumulative failure rate of 1% [F (t)=1%] along the vertical axis. The solid line shows the power cycling lifetime of the conventional package equipped with Si devices and the plot (○) is the lifetime verified with the new package equipped with Si devices. This result shows that, with the test condition ΔT_j=150 °C, the new package is expected to offer a lifetime more than ten times longer than that of the conventional package.

Accordingly, implantation and epitaxial metal oxide semiconductor (IEMOS), which is the SiC-MOSFET jointly developed with the National Institute of Advanced Industrial Science and Technology, has been mounted in the new package to conduct a power cycling test with ΔT_j=150 °C. The test result confirmed that 50,000 cycles with F (t) = 1%, a lifetime improved by more than 20 times from the conventional package equipped with Si devices, has been achieved[1] (see plot ● in Fig. 6). With the conventional package, breakage such as separation of the chip electrode from wire bonding occurs as the operation temperature increases, and this reduces the lifetime[2]. Meanwhile, the new package is encapsulated in epoxy resin with high heat resistance and breakage of junction between the chip electrode and copper pin is restrained by mitigating the thermal stress generated during operation. In addition, an epoxy resin with a glass transition temperature T_g of 200 °C or higher has been developed[3], which limits variations in mechanical and physical properties such as linear expansion coefficient and elastic modulus to a certain extent within the range of operating temperature and achieves high reliability.

(2) ΔT_c power cycling test

For mounting in a PCS for photovoltaic power generation (solar PCS) of a mega-solar plant, etc., the operation modes must be grasped to conduct a reliability test. A solar PCS operates in continuous mode during power generation in the daytime and stops during the night-time. To verify the thermal load on the module in that process, it is also important to conduct a ΔT_c power cycling test with a varying module surface temperature T_c during operation.

Figure 7 shows a scanning acoustic tomograph image of a sample subjected to a ΔT_c power cycling test with the conventional package structure. After 20,000 cycles, breakage is generated in the solder bonding between the copper base and DCB substrate, which is not observed before the test, and the thermal resistance is estimated to have increased and caused the failure. With the new package, however, the structure does not include a copper base and the types of failure seen with the conventional package are unlikely but the durability of the junction between the isolation substrate and the chip has an impact on the lifetime in the ΔT_c power cycling test. Given this factor, with the test starting temperature of 25 °C and the ΔT_c=80 °C condition, changes in the thermal resistance of the new package in the ΔT_c power cycling test have been verified (see Fig. 8). Thermal resistance along the vertical axis is based on the initial values of the respective samples to show variations. The result shows that, variations in the thermal resistance are confined within 7% of the initial values even after 25,000 cycles and no increasing tendency is observed.

Figure 9 shows a scanning acoustic tomograph image of the chip bottom junction of the package before

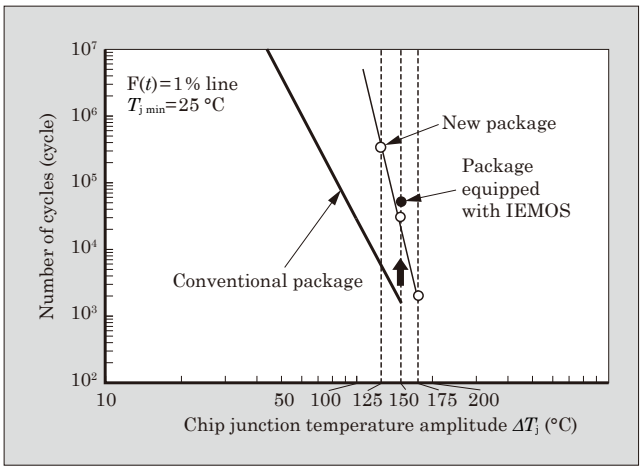

Fig.6 ΔT_j power cycling test lifetime

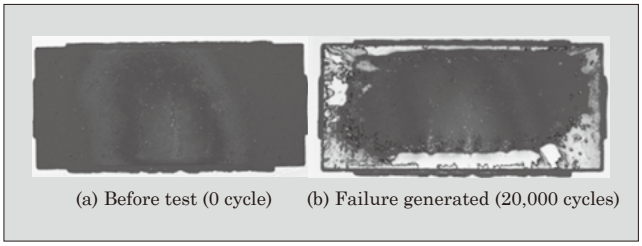

Fig.7 Scanning acoustic tomograph image of conventional package structure in ΔT_c power cycling test

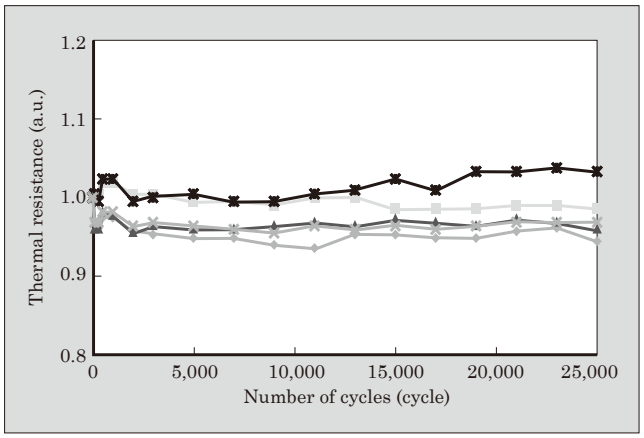

Fig.8 Changes in thermal resistance of new package structure in ΔT_c power cycling test

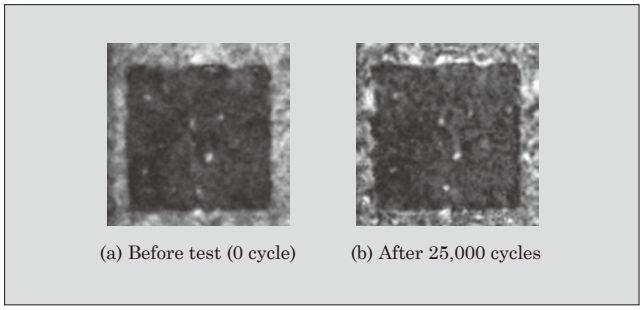

Fig.9 Scanning acoustic tomograph image of chip bottom solder bonding in ΔT_c power cycling test

and after the ΔT_c power cycling test. As compared with before the test, no change in the bonding condition has been observed even after 25,000 cycles. In addition, no crack in the ceramic substrate or separation of the thick copper block is observed, which confirms that the new package has sufficient durability for application to a PCS.

3. Application to Power Conditioner for Mega-Solar Plants

In mega-solar plants or other types of photovoltaic power generation, the DC voltage generated in photovoltaic cells is converted into AC voltage by PCS for transmission. Photovoltaic power generation has an issue of reduced conversion efficiency of the PCS due to a voltage reduction caused by a decrease in insolation or rise in temperature. One solution is to equip the PCS with a booster circuit (chopper circuit). This method makes it possible to raise the minimum input voltage to the inverter for conversion into AC voltage, which improves the AC voltage output along with the rise in the minimum input voltage. By applying the SiC devices to the booster circuit, generated loss of the boost converter can be suppressed, and this raises expectations for an improvement in the conversion efficiency of the entire PCS including the inverter. Furthermore, the boost converter, which requires a volume equivalent to that of the inverter with the conventional Si devices, can be miniaturized by using SiC devices. Accordingly, we have applied the new package described up to now to develop an all-SiC chopper module for booster circuits that uses the features of SiC devices (see Fig. 10).

The SiC devices mounted in the all-SiC chopper module are IEMOS and SiC-SBD, jointly developed with the National Institute of Advanced Industrial Science and Technology, and they are mass-produced at our Matsumoto Factory (see Fig. 11). Figure 12 shows the appearance of the PCS for mega-solar plants equipped with this all-SiC chopper module. It measures 2,980×900×1,900 (mm) and realizes an output apparent power of 1,000 kW, which is among the

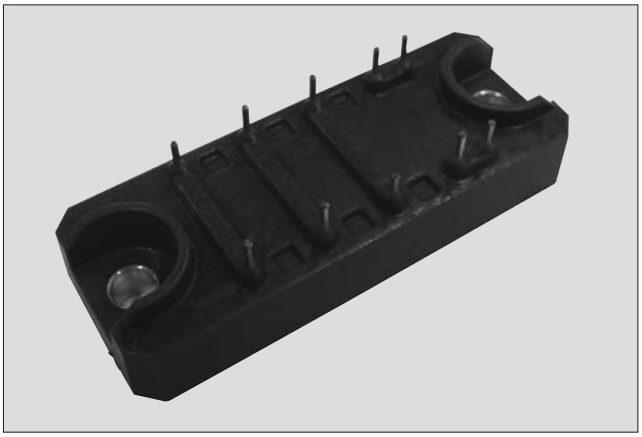

Fig.10 All-SiC chopper module

Fig.11 6-inch SiC wafer

Fig.12 Power conditioner for mega-solar plants

world's highest as an indoor system. By applying the all-SiC chopper module that has been developed to the booster circuit, the loss has been successfully reduced and the world's highest-class PCS conversion efficiency of 98.8% has been achieved (98.5% with the conventional product)[4]. In addition, circuit miniaturization has also been realized to achieve a 20% size reduction from the conventional switchboard, which contributes to a reduction in installation costs including transportation cost.

4. Postscript

We have developed an all-SiC chopper module for PCS for mega-solar plants, achieved the world's highest-class conversion efficiency of 98.8%, which was difficult with Si devices, and realized miniaturization of equipment.

In the future, we intend to contribute to the realization of a low carbon society by applying the all-SiC module to various power electronics devices to improve energy utilization efficiency.

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