**ProASIC3E Flash Family FPGAs with Optional Soft ARM® Support**

### Features and Benefits

#### High Capacity
- 600 k to 3 Million System Gates
- 108 to 504 kbits of True Dual-Port SRAM
- Up to 620 User I/Os

#### Reprogrammable Flash Technology
- 130-nm, 7-Layer Metal (6 Copper), Flash-Based CMOS Process
- Live at Power-Up (LAPU) Level 0 Support
- Single-Chip Solution
- Retains Programmed Design when Powered Off

#### On-Chip User Nonvolatile Memory
- 1 kbit of FlashROM with Synchronous Interfacing

#### High Performance
- 350 MHz System Performance
- 3.3 V, 66 MHz 64-Bit PCI

#### In-System Programming (ISP) and Security
- FlashLock® to Secure FPGA Contents

#### Low Power
- Core Voltage for Low Power
- Support for 1.5 V-Only Systems
- Low-Impedance Flash Switches

#### High-Performance Routing Hierarchy
- Segmented, Hierarchical Routing and Clock Structure
- Ultra-Fast Local and Long-Line Network
- Enhanced High-Speed, Very-Long-Line Network
- High-Performance, Low-Skew Global Network
- Architecture Supports Ultra-High Utilization

#### Pro (Professional) I/O
- 700 Mbps DDR, LVDS-Capable I/Os

- 1.5 V, 1.8 V, 2.5 V, and 3.3 V Mixed-Voltage Operation
- Bank-Selectable I/O Voltages—up to 8 Banks per Chip
- Single-Ended I/O Standards: LVTTL, LVCMOS 3.3 V / 2.5 V / 1.8 V / 1.5 V, 3.3 V  PCI / 3.3 V PCI-X, and  LVCMOS 2.5 V / 5.0 V Input
- Differential I/O Standards: LVPECL, LVDS, B-LVDS, and M-LVDS
- Voltage-Referenced I/O Standards: GTL+ 2.5 V / 3.3 V, GTL 2.5 V / 3.3 V, HSTL Class I and II, SSTL2 Class I and II, SSTL3 Class I and II
- I/O Registers on Input, Output, and Enable Paths
- Hot-Swappable and Cold Sparing I/Os
- Programmable Output Slew Rate and Drive Strength
- Programmable Input Delay
- Schmitt Trigger Option on Single-Ended Inputs
- Weak Pull-Up/Down
- IEEE 1149.1 (JTAG) Boundary Scan Test
- Pin-Compatible Packages across the ProASIC®3E Family

#### Clock Conditioning Circuit (CCC) and PLL
- Six CCC Blocks, Each with an Integrated PLL
- Configurable Phase-Shift, Multiply/Divide, Delay Capacities and External Feedback
- Wide Input Frequency Range (1.5 MHz to 200 MHz)

#### SRAMs and FIFOs
- Variable-Aspect-Ratio 4,608-Bit RAM Blocks (×1, ×2, ×4, ×9, and ×18 organizations available)
- True Dual-Port SRAM (except ×18)
- 24 SRAM and FIFO Configurations with Synchronous Operation up to 350 MHz

#### ARM Processor Support in ProASIC3E FPGAs
- M1 ProASIC3E Devices—Cortex-M1 Soft Processor Available with or without Debug

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### Table 1-1 • ProASIC3E Product Family

<table>
<thead>
<tr>
<th>ProASIC3E Devices</th>
<th>A3PE600</th>
<th>A3PE1500</th>
<th>A3PE3000</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cortex-M1 Devices 1</td>
<td></td>
<td>M1A3PE1500</td>
<td>M1A3PE3000</td>
</tr>
<tr>
<td>System Gates</td>
<td>600 k</td>
<td>1.5 M</td>
<td>3 M</td>
</tr>
<tr>
<td>VersaTiles (D-flip-flops)</td>
<td>13,824</td>
<td>38,400</td>
<td>75,264</td>
</tr>
<tr>
<td>RAM kbits (1,024 bits)</td>
<td>108</td>
<td>270</td>
<td>504</td>
</tr>
<tr>
<td>4,608-Bit Blocks</td>
<td>24</td>
<td>60</td>
<td>112</td>
</tr>
<tr>
<td>FlashROM Bits</td>
<td>1 k</td>
<td>1 k</td>
<td>1 k</td>
</tr>
<tr>
<td>Secure (AES) ISP</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>CCCs with Integrated PLLs 2</td>
<td>6</td>
<td>6</td>
<td>6</td>
</tr>
<tr>
<td>VersaNet Globals 3</td>
<td>18</td>
<td>18</td>
<td>18</td>
</tr>
<tr>
<td>I/O Banks</td>
<td>8</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>Maximum User I/Os</td>
<td>270</td>
<td>444</td>
<td>620</td>
</tr>
<tr>
<td>Package Pins</td>
<td>PQ208</td>
<td>PQ208</td>
<td>PQ208</td>
</tr>
<tr>
<td></td>
<td>FG256, FG484</td>
<td>FG484, FG676</td>
<td>FG324, FG484, FG896</td>
</tr>
</tbody>
</table>

**Notes:**
1. Refer to the Cortex-M1 product brief for more information.
2. The PQ208 package supports six CCCs and two PLLs.
3. Six chip (main) and three quadrant global networks are available.
4. For devices supporting lower densities, refer to the ProASIC3 Flash Family FPGAs handbook.
## I/Os Per Package

<table>
<thead>
<tr>
<th>ProASIC3E Devices</th>
<th>A3PE600</th>
<th>A3PE1500</th>
<th>A3PE3000</th>
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</thead>
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<tr>
<td>Cortex-M1 Devices</td>
<td></td>
<td>M1A3PE1500</td>
<td>M1A3PE3000</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>PQ208</td>
<td>147</td>
<td>65</td>
<td>147</td>
<td>65</td>
<td>147</td>
<td>65</td>
</tr>
<tr>
<td>FG256</td>
<td>165</td>
<td>79</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>FG324</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>221</td>
<td>110</td>
</tr>
<tr>
<td>FG484</td>
<td>270</td>
<td>135</td>
<td>280</td>
<td>139</td>
<td>341</td>
<td>168</td>
</tr>
<tr>
<td>FG676</td>
<td>–</td>
<td>–</td>
<td>444</td>
<td>222</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>FG896</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>620</td>
<td>310</td>
</tr>
</tbody>
</table>

**Notes:**

1. When considering migrating your design to a lower- or higher-density device, refer to the ProASIC3E Flash Family FPGAs handbook to ensure compliance with design and board migration requirements.
2. Each used differential I/O pair reduces the number of single-ended I/Os available by two.
3. For A3PE1500 and A3PE3000 devices, the usage of certain I/O standards is limited as follows:
   - SSTL3(I) and (II): up to 40 I/Os per north or south bank
   - LVPECL / GTL+ 3.3 V / GTL 3.3 V: up to 48 I/Os per north or south bank
   - SSTL2(I) and (II) / GTL+ 2.5 V / GTL 2.5 V: up to 72 I/Os per north or south bank
4. FG256 and FG484 are footprint-compatible packages.
5. When using voltage-referenced I/O standards, one I/O pin should be assigned as a voltage-referenced pin (V_REF) per minibank (group of I/Os).
6. "G" indicates RoHS-compliant packages. Refer to the "ProASIC3E Ordering Information" on page III for the location of the "G" in the part number.

### Table 1-2 • ProASIC3E FPGAs Package Sizes Dimensions

<table>
<thead>
<tr>
<th>Package</th>
<th>PQ208</th>
<th>FG256</th>
<th>FG324</th>
<th>FG484</th>
<th>FG676</th>
<th>FG896</th>
</tr>
</thead>
<tbody>
<tr>
<td>Length × Width (mm × mm)</td>
<td>28 × 28</td>
<td>17 × 17</td>
<td>19 × 19</td>
<td>23 × 23</td>
<td>27 × 27</td>
<td>31 × 31</td>
</tr>
<tr>
<td>Nominal Area (mm²)</td>
<td>784</td>
<td>289</td>
<td>361</td>
<td>529</td>
<td>729</td>
<td>961</td>
</tr>
<tr>
<td>Pitch (mm)</td>
<td>0.5</td>
<td>1.0</td>
<td>1.0</td>
<td>1.0</td>
<td>1.0</td>
<td>1.0</td>
</tr>
<tr>
<td>Height (mm)</td>
<td>3.40</td>
<td>1.60</td>
<td>1.63</td>
<td>2.23</td>
<td>2.23</td>
<td>2.23</td>
</tr>
</tbody>
</table>
## ProASIC3E Ordering Information

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Speed Grade</th>
<th>Package Lead Count</th>
<th>Package Type</th>
<th>Lead-Free Packaging</th>
<th>Application (Temperature Range)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A3PE3000</td>
<td>1</td>
<td>FG</td>
<td>G</td>
<td>896</td>
<td>Blank = Commercial (0°C to +70°C Ambient Temperature)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>I = Industrial (–40°C to +85°C Ambient Temperature)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>PP = Pre-Production</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ES = Engineering Sample (Room Temperature Only)</td>
</tr>
</tbody>
</table>

**Part Number**

- **ProASIC3E Devices**
  - A3PE600 = 600,000 System Gates
  - A3PE1500 = 1,500,000 System Gates
  - A3PE3000 = 3,000,000 System Gates

- **ProASIC3E Devices with Cortex-M1**
  - M1A3PE1500 = 1,500,000 System Gates
  - M1A3PE3000 = 3,000,000 System Gates
## Temperature Grade Offerings

<table>
<thead>
<tr>
<th>Package</th>
<th>A3PE600</th>
<th>A3PE1500</th>
<th>A3PE3000</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cortex-M1 Devices</td>
<td></td>
<td>M1A3PE1500</td>
<td>M1A3PE3000</td>
</tr>
<tr>
<td>PQ208</td>
<td>C, I</td>
<td>C, I</td>
<td>C, I</td>
</tr>
<tr>
<td>FG256</td>
<td>C, I</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>FG324</td>
<td>–</td>
<td>–</td>
<td>C, I</td>
</tr>
<tr>
<td>FG484</td>
<td>C, I</td>
<td>C, I</td>
<td>C, I</td>
</tr>
<tr>
<td>FG676</td>
<td>–</td>
<td>C, I</td>
<td>–</td>
</tr>
<tr>
<td>FG896</td>
<td>–</td>
<td>–</td>
<td>C, I</td>
</tr>
</tbody>
</table>

**Note:**  
C = Commercial temperature range: 0°C to 70°C ambient temperature  
I = Industrial temperature range: –40°C to 85°C ambient temperature

## Speed Grade and Temperature Grade Matrix

<table>
<thead>
<tr>
<th>Temperature Grade</th>
<th>Std.</th>
<th>–1</th>
<th>–2</th>
</tr>
</thead>
<tbody>
<tr>
<td>C&lt;sup&gt;1&lt;/sup&gt;</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>I&lt;sup&gt;2&lt;/sup&gt;</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>

**Notes:**

1. C = Commercial temperature range: 0°C to 70°C ambient temperature
2. I = Industrial temperature range: –40°C to 85°C ambient temperature

References made to ProASIC3E devices also apply to ARM-enabled ProASIC3E devices. The ARM-enabled part numbers start with M1 (Cortex-M1).

Contact your local Actel representative for device availability:  
1 – ProASIC3E Device Family Overview

General Description

ProASIC3E, the third-generation family of Actel flash FPGAs, offers performance, density, and features beyond those of the ProASICPLUS® family. Nonvolatile flash technology gives ProASIC3E devices the advantage of being a secure, low-power, single-chip solution that is live at power-up (LAPU). ProASIC3E is reprogrammable and offers time-to-market benefits at an ASIC-level unit cost. These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

ProASIC3E devices offer 1 kbit of on-chip, programmable, nonvolatile FlashROM storage as well as clock conditioning circuitry based on six integrated phase-locked loops (PLLs). ProASIC3E devices have up to three million system gates, supported with up to 504 kbits of true dual-port SRAM and up to 620 user I/Os.

Several ProASIC3E devices support the Cortex-M1 soft IP cores, and the ARM-Enabled devices have Actel ordering numbers that begin with M1A3PE.

Flash Advantages

Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, performance, and ease of use. Unlike SRAM-based FPGAs, flash-based ProASIC3E devices allow all functionality to be live at power-up; no external boot PROM is required. On-board security mechanisms prevent access to all the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system reprogramming to support future design iterations and field upgrades with confidence that valuable intellectual property (IP) cannot be compromised or copied. Secure ISP can be performed using the industry-standard AES algorithm. The ProASIC3E family device architecture mitigates the need for ASIC migration at higher user volumes. This makes the ProASIC3E family a cost-effective ASIC replacement solution, especially for applications in the consumer, networking/communications, computing, and avionics markets.

Security

The nonvolatile, flash-based ProASIC3E devices do not require a boot PROM, so there is no vulnerable external bitstream that can be easily copied. ProASIC3E devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

ProASIC3E devices utilize a 128-bit flash-based lock and a separate AES key to secure programmed intellectual property and configuration data. In addition, all FlashROM data in ProASIC3E devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. The AES standard was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the 1977 DES standard. ProASIC3E devices have a built-in AES decryption engine and a flash-based AES key that make them the most comprehensive programmable logic device security solution available today. ProASIC3E devices with AES-based security allow for secure, remote field updates over public networks such as the Internet, and ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves. The contents of a programmed ProASIC3E device cannot be read back, although secure design verification is possible.

Security, built into the FPGA fabric, is an inherent component of the ProASIC3E family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. The ProASIC3E family, with FlashLock and AES security, is unique in being highly resistant to both invasive and noninvasive attacks. Your
valuable IP is protected and secure, making remote ISP possible. A ProASIC3E device provides the most impenetrable security for programmable logic designs.

**Single Chip**

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based ProASIC3E FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

**Live at Power-Up**

The Actel flash-based ProASIC3E devices support Level 0 of the LAPU classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The LAPU feature of flash-based ProASIC3E devices greatly simplifies total system design and reduces total system cost, often eliminating the need for CPLDs and clock generation PLLs that are used for these purposes in a system. In addition, glitches and brownouts in system power will not corrupt the ProASIC3E device's flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based ProASIC3E devices simplify total system design and reduce cost and design risk while increasing system reliability and improving system initialization time.

**Firm Errors**

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of ProASIC3E flash-based FPGAs. Once it is programmed, the flash cell configuration element of ProASIC3E FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

**Low Power**

Flash-based ProASIC3E devices exhibit power characteristics similar to an ASIC, making them an ideal choice for power-sensitive applications. ProASIC3E devices have only a very limited power-on current surge and no high-current transition period, both of which occur on many FPGAs. ProASIC3E devices also have low dynamic power consumption to further maximize power savings.

**Advanced Flash Technology**

The ProASIC3E family offers many benefits, including nonvolatility and reprogrammability through an advanced flash-based, 130-nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.
Advanced Architecture

The proprietary ProASIC3E architecture provides granularity comparable to standard-cell ASICs. The ProASIC3E device consists of five distinct and programmable architectural features (Figure 1-1 on page 3):

- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory
- Extensive CCCs and PLLs
- Pro I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the ProASIC3E core tile as either a three-input lookup table (LUT) equivalent or as a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the Actel ProASIC family of third-generation architecture Flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

In addition, extensive on-chip programming circuitry allows for rapid, single-voltage (3.3 V) programming of ProASIC3E devices via an IEEE 1532 JTAG interface.

Figure 1-1 • ProASIC3E Device Architecture Overview
**VersaTiles**

The ProASIC3E core consists of VersaTiles, which have been enhanced beyond the ProASIC PLUS® core tiles. The ProASIC3E VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

Refer to Figure 1-2 for VersaTile configurations.

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**User Nonvolatile FlashROM**

Actel ProASIC3E devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard ProASIC3E IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks, as in security keys stored in the FlashROM for a user design.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The Actel ProASIC3E development software solutions, Libero® Integrated Design Environment (IDE) and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Actel Libero IDE and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.
SRAM and FIFO

ProASIC3E devices have embedded SRAM blocks along their north and south sides. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro.

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

PLL and CCC

ProASIC3E devices provide designers with very flexible clock conditioning capabilities. Each member of the ProASIC3E family contains six CCCs, each with an integrated PLL.

The six CCC blocks are located at the four corners and the centers of the east and west sides.

To maximize user I/Os, only the center east and west PLLs are available in devices using the PQ208 package. However, all six CCC blocks are still usable; the four corner CCCs allow simple clock delay operations as well as clock spine access.

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several inputs located near the CCC that have dedicated connections to the CCC block.

The CCC block has these key features:

- Wide input frequency range \( f_{IN_{CCC}} \) = 1.5 MHz to 350 MHz
- Output frequency range \( f_{OUT_{CCC}} \) = 0.75 MHz to 350 MHz
- Clock delay adjustment via programmable and fixed delays from –7.56 ns to +11.12 ns
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°. Output phase shift depends on the output divider configuration.
- Output duty cycle = 50% ± 1.5% or better
- Low output jitter: worst case < 2.5% × clock period peak-to-peak period jitter when single global network used
- Maximum acquisition time = 300 µs
- Low power consumption of 5 mW
- Exceptional tolerance to input period jitter— allowable input jitter is up to 1.5 ns
- Four precise phases; maximum misalignment between adjacent phases of 40 ps × (350 MHz / \( f_{OUT_{CCC}} \))

Global Clocking

ProASIC3E devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high fanout nets.
Pro I/Os with Advanced I/O Standards

The ProASIC3E family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V). ProASIC3E FPGAs support 19 different I/O standards, including single-ended, differential, and voltage-referenced. The I/Os are organized into banks, with eight banks per device (two per side). The configuration of these banks determines the I/O standards supported. Each I/O bank is subdivided into VREF minibanks, which are used by voltage-referenced I/Os. VREF minibanks contain 8 to 18 I/Os. All the I/Os in a given minibank share a common VREF line. Therefore, if any I/O in a given VREF minibank is configured as a VREF pin, the remaining I/Os in that minibank will be able to use that reference voltage.

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following:

- Single-Data-Rate applications (e.g., PCI 66 MHz, bidirectional SSTL 2 and 3, Class I and II)
- Double-Data-Rate applications (e.g., DDR LVDS, B-LVDS, and M-LVDS I/Os for point-to-point communications, and DDR 200 MHz SRAM using bidirectional HSTL Class II)

ProASIC3E banks support M-LVDS with 20 multi-drop points.

Hot-swap (also called hot-plug, or hot-insertion) is the operation of hot-insertion or hot-removal of a card in a powered-up system.

Cold-sparing (also called cold-swap) refers to the ability of a device to leave system data undisturbed when the system is powered up, while the component itself is powered down, or when power supplies are floating.
**Part Number and Revision Date**

Part Number 51700098-001-3
Revised August 2009

**List of Changes**

The following table lists critical changes that were made in the current version of the document.

<table>
<thead>
<tr>
<th>Previous Version</th>
<th>Changes in Current Version (v1.2)</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>v1.1 (February 2009)</td>
<td>All references to speed grade –F have been removed from this document. The &quot;Pro I/Os with Advanced I/O Standards&quot; section was revised to add definitions of hot-swap and cold-sparing.</td>
<td>N/A</td>
</tr>
<tr>
<td>v1.0 (March 2008)</td>
<td>Table 1-2 · ProASIC3E FPGAs Package Sizes Dimensions is new.</td>
<td>II</td>
</tr>
<tr>
<td>51700098-001-1 (January 2008)</td>
<td>This document was divided into two sections and given a version number, starting at v1.0. The first section of the document includes features, benefits, ordering information, and temperature and speed grade offerings. The second section is a device family overview.</td>
<td>N/A</td>
</tr>
<tr>
<td>51700098-001-0 (January 2008)</td>
<td>The FG324 package was added to the &quot;ProASIC3E Product Family&quot; table, the &quot;I/Os Per Package&quot; table, and the &quot;Temperature Grade Offerings&quot; table for A3PE3000.</td>
<td>I, II, IV</td>
</tr>
<tr>
<td>v2.1 (July 2007)</td>
<td>This document was previously in datasheet v2.1. As a result of moving to the handbook format, Actel has restarted the version numbers. The new version number is 51700098-001-0.</td>
<td>N/A</td>
</tr>
<tr>
<td>v2.0 (April 2007)</td>
<td>CoreMP7 information was removed from the &quot;Features and Benefits&quot; section. CoreMP7 information was removed from the &quot;Features and Benefits&quot; section.</td>
<td>i</td>
</tr>
<tr>
<td>Advance v0.6 (January 2007)</td>
<td>The M1 device part numbers have been updated in Table 4 · ProASIC3E Product Family, &quot;Packaging Tables&quot;, &quot;Temperature Grade Offerings&quot;, &quot;Speed Grade and Temperature Grade Matrix&quot;, and &quot;Speed Grade and Temperature Grade Matrix&quot;. The words &quot;ambient temperature&quot; were added to the temperature range in the &quot;Temperature Grade Offerings&quot;, &quot;Speed Grade and Temperature Grade Matrix&quot;, and &quot;Speed Grade and Temperature Grade Matrix&quot; sections. The &quot;Clock Conditioning Circuit (CCC) and PLL&quot; section was updated.</td>
<td>ii, iii, iv, iv</td>
</tr>
<tr>
<td>Advance v0.5 (April 2006)</td>
<td>In the &quot;Packaging Tables&quot; table, the number of I/Os for the A3PE1500 was changed for the FG484 and FG766 packages.</td>
<td>iii</td>
</tr>
<tr>
<td>Advance v0.4 (October 2005)</td>
<td>B-LVDS and M-LDVS are new I/O standards added to the datasheet. The term flow-through was changed to pass-through.</td>
<td>N/A</td>
</tr>
<tr>
<td>Advance v0.2</td>
<td>The &quot;Packaging Tables&quot; table was updated.</td>
<td>ii</td>
</tr>
</tbody>
</table>
Datasheet Categories

Categories
In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advance," "Preliminary," and "Production." The definitions of these categories are as follows:

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The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance
This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary
The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Unmarked (production)
This version contains information that is considered to be final.

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